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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,192	01/22/2004	Masao Shinozaki	XA-9590A	3099

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
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EXAMINER	
WOJCIECHOWICZ, EDWARD JOSEPH	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,192	SHINOZAKI ET AL.	
	Examiner	Art Unit	
	Edward Wojciechowicz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 8-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 8-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1-22-04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Icel et al (5,248,624). The reference to Icel teaches all of the elements of the claimed process. For example, Icel describes the formation of plural types of MOS transistors, referred to by Icel as Poly 1 transistors and Poly 2 transistors, which also include both NMOS and PMOS transistors which would of necessity use different power supply voltages, where a first process common to both types of transistors is performed, such as the formation of N-well region (13), which is described at col. 7, l. 10-15. After which a second process, which is different for each type of transistor is performed. This second process is comprised, for example, by the formation of different gate oxide thickness (76) and (77) for the Poly 1 and Poly2 transistors, as discussed at col. 4, l. 56-64.

Furthermore, as can be seen in Fig. 1B and Fig. 2 of Icel, after these different gate dielectrics are formed, additional, or third processes, common to both types of transistors, would necessarily be performed in order to complete the devices. A common third process would be used, for example, to form such elements as the gate electrodes and the surface passivation layers such as element (21). Similarly, certain

active areas of active regions, such as some of the source and drain regions, are also formed equal to each other.

In addition to teaching that the gate dielectrics may be formed with different thicknesses, in a second process that is different for the different types of transistors, Icel also discloses other device parameters that would inherently be of different values, and consequently require a different process to form. For example, the EEPROM devices have floating gates which are formed to be longer than other gates of the device. See, for example, Fig. 3 where floating gate (45) is formed to be longer than floating gate (30). Similarly, Icel also teaches a second process where different channels having inherently different channel impurity concentrations are formed, such as the devices formed with LDD regions in the channel. See, for example, NMOS device (68) in Fig. 1B. Icel also discloses (col. 1, l. 17) that this type of device can be used in output circuits.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Icel in view of Esses (6,130,173). While Icel teaches the basic inventive process of forming different MOS devices with some common process steps, and with some

different process steps, he does not explicitly apply this concept to processing separate first and second semiconductor wafers. Esses, however, does teach this feature of using some common processes applied to multiple wafers, and then applying different processes to different wafers in order to form MOS transistors with different parameters. For example, as shown in Fig. 3, Esses processes different wafers with some common processes such as a blanket deposition of polysilicon gate material (col. 2, l. 15) and then proceeds to purposely vary certain parameters, such as gate length, in a second process step.

Esses also teaches that after the different process steps are applied, additional conventional processing steps may be applied to all of the wafers (col. 8, l.9-12). In addition, the limitations of claim 20 would be directly related to the selection of the gate length, and is also within the scope of Esses's teaching that other device parameters may also be varied using his inventive process (col. 9, l.33-35).

One skilled in the art would be motivated to combine these references in order to gain increased processing efficiency by applying the specific device tailoring performed by Icel on a single chip to much larger wafers, as taught by Esses.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Wojciechowicz whose telephone number is (571) 272-1739. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edward Wojciechowicz
Primary Examiner
Art Unit 2815

EW: ew